What is claimed is:

1. A method of transmitting digital information, comprising the steps of:

(a) transmitting a first word of a packet, comprising the steps of:

(1) transmitting start information onto a first bus, wherein the start information indicates a start of the packet;

(2) transmitting lower order memory address bits onto a first group of second bus lines;

(3) transmitting first opcode information onto an Nth bus line of the second bus lines, wherein N is an integer, and wherein the Nth bus line is not a bus line within the first group of the second bus lines;

(b) transmitting a second word of the packet, comprising the steps of:

(1) transmitting second op code onto the first bus;

(2) transmitting higher order memory address bits onto the first group of the second bus lines;

(3) transmitting third op code information onto the Nth bus line of the second bus lines.

2. The method of claim 1 of transmitting digital information, further comprising the steps of:

(a) transmitting a third word of a packet, comprising the steps of:

(1) transmitting a master device code for detecting collisions;

(2) transmitting count information for determining a count of a number of bytes of a memory transaction.

3. In a digital system comprising a master device and at least one memory device, a process for transmitting memory requests to the memory device comprising the steps of:

transmitting a first word of a packet, comprising the steps of:

transmitting start information onto a first bus line, said start information indicating the start of the packet,

transmitting a first portion of a lower order memory address bits onto a first group of second bus lines, said lower order memory bits comprising information to perform page mode memory accesses, and transmitting a first portion of op code information onto a second group of the second bus lines; and

transmitting a second word of the packet, comprising the steps of:

transmitting a second portion of op code information onto the first bus line, transmitting a third portion of op code information onto the second group of the second bus lines, wherein an op code for page mode accesses can be detected from said first, second and third portions of op code information; and

transmitting a second portion of the lower order memory address bits onto the first group of the second bus lines;

wherein page mode access can be performed after transmission of the second word of the packet.

4. In a computer system comprising a master device and at least one memory device, a bus system for transmitting memory requests to the memory device comprising:

a plurality of bus lines for transmission of memory requests;

a packet comprising a memory request for transmission across the bus lines, said packet comprising:

a first word comprising:

start information indicating the start of the packet;

a first portion of lower order memory address bits comprising information to perform page mode memory accesses; and

a first portion of op code information; and

a second word comprising:

a second and third portion of op code information, wherein an op code for page mode accesses can be detected from the first, second and third portions of op code information, and

a second portion of the lower order memory address bits;

wherein page mode access can be performed after transmission of the second word of the packet.

5. The bus system as set forth in claim 4 wherein said start information is located at a predetermined location in the first word of the packet, said system further comprising:

means for monitoring the predetermined location in each word during transmission of subsequent words of the packet for information other than the start of the packet; and

means for detecting a collision if information occurs at the predetermined location in subsequent words of the packet, said information occurring due to the start information of a second packet overlapping the first packet.

6. The bus system as forth in claim 5, wherein said packet further comprises a code identifying the device transmitting the packet, said means for detecting a collision further comprising means for detecting the code to determine where the code is valid, an invalid code resulting from a collision of packets.

7. The bus system as set forth in claim 4, wherein said packet further comprises count information indicating the number of bytes of memory to be transmitted across the bus lines during the memory transaction requested.

8. The bus system as set forth in claim 7, wherein said data is transmitted in a multiple byte block format, said system further comprising:

means for generating a first mask for the first multiple byte block of the data to be transmitted, said mask indicating the bytes of the multiple byte block which are part of the memory operation requested; and

means for generating a second mask for the last multiple byte block, said mask indicating the bytes of the last multiple byte block which are part of the memory operation requested.

9. The bus system as set forth in claim 8, wherein data is transmitted in 4 byte blocks, the first mask is generated from the two least significant bits of the address bits and the second mask is generated from the two least significant bits of the count information.

10. The bus system as set forth in claim 8, further comprising a first and second look up table comprising mask patterns, said masks generated by performing a table lookup respectively using the address bits and the count information.

11. The bus system as set forth in claim 4, further comprising a summing means for summing the two least significant address bits and internal byte count to produce an overflow value and count information, said overflow information indicating that although the size of the data of the memory request is less than the maximum number of bytes allowed in the memory operation, the granularity of the multiple byte block format transmitted acres the bus prohibits the transaction and the request should be separated into two separate memory requests.

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